Remote FPGA Upgrades with Fail-Safe Booting

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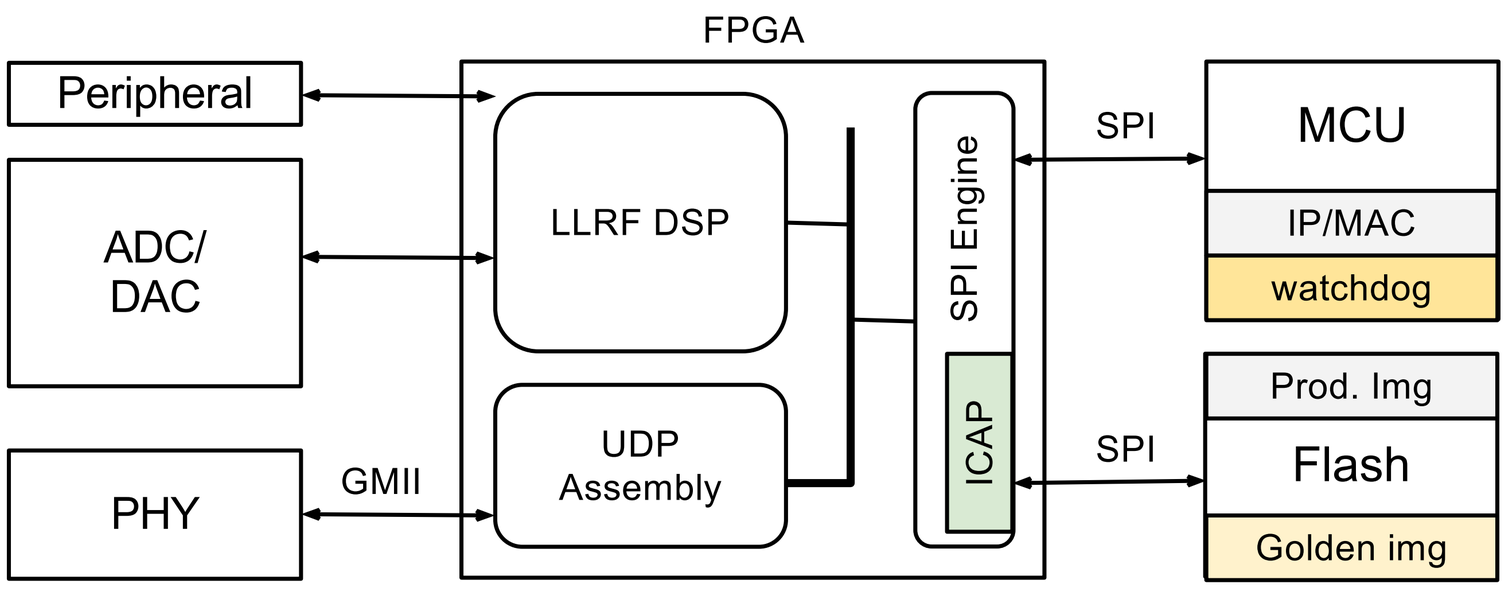
Abstract

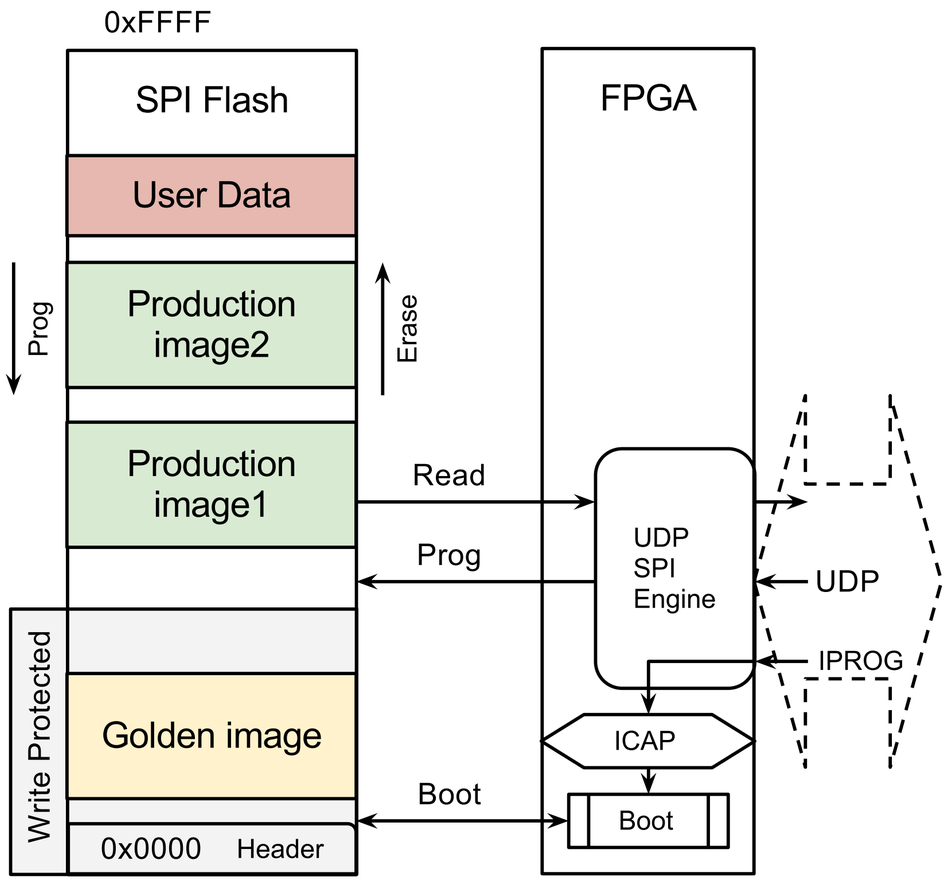
Future LLRF controllers can benefit from direct access to their digital signal processing fabric via a gigabit Ethernet (GBE) communication interface. That GBE interface can be implemented within most mainstream FPGAs, connecting a high-performance on-chip bus to a well-understood and widely deployed network backbone. Since the LLRF hardware is expected to run unattended, in a remote location, for decades, and still support gateware upgrades and bugfixes, it is important for the remote administration process to have a firm foundation. This administration, including the in-place upgrading of gateware, should take place through GBE, to avoid additional accelerator-wide cabling. This paper demonstrates a fail-safe remote upgrade scheme consisting of a UDP packet switch engine, an SPI flash interface, and an MCU watchdog.

System setup



Test Hardware	Xilinx SP601
FPGA	Spartan 6 LX45
MCU	STM32
SPI Flash	Winbond W25Q64BV
UDP Engine	LBNL PSPEPS

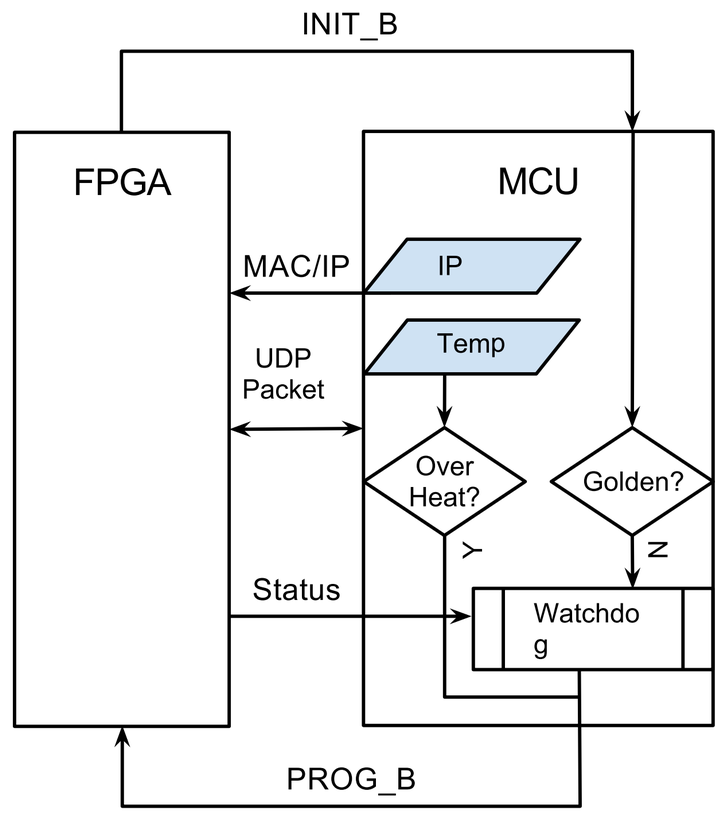
FPGA Remote Upgrade



Features:

- Multiple boot images with section write-protection for golden image
- Remote read SPI flash
- Remote program SPI flash
- SPIx2/QSPI support
- Remote IPROG reconfiguration using ICAP
  - Remote rebooting
  - Selection of production images
  - Spartan6 Multiboot logic support

Failsafe booting



- Read/Write UDP packet to/from SPI
- Set FPGA IP& MAC address from SPI
- Watchdog response timeout
- PROG_B reboot FPGA to guarantee golden
- Monitor INIT_B to determine golden
- Temperature monitoring and overheat shutdown

Conclusions

- 2.12 s to program a 453.5 K bytes image by SPIx2.
- Remote recognition of bit file git version tag.